CLAIMS

I claim:

1. A discrete decoupling capacitor structure for reducing stray inductance in a circuit structure, which circuit structure includes: a printed circuit board having first and second opposite faces and at least two voltage planes, and vias extending from each of said faces to one of said voltage planes, an I/C chip structure having at least one active device thereon, connectors connecting said active devices on said I/C chip structure to said vias on one face of said printed circuit board, said decoupling capacitor structure comprising:

at least two interlaced conductive plates in dielectric material forming at least one capacitor,

vias extending from each of said conductive plates through said dielectric material to connect each via to a circuit board via on said second face of said printed circuit board,

said vias in said decoupling capacitor structure being parallel to each other and each via connected to one conductive plate being located adjacent a via connected to another conductive plate.

2. The invention as defined in claim 1 wherein said vias in said printed circuit board are arranged in the same pattern as the vias in said decoupling capacitor.

3. The invention as defined in claim 2 wherein said I/C chip structure has vias therein arranged in the same pattern as the pattern of the vias in said decoupling capacitor, and each of said vias arranged in said pattern in said I/C chip structure being connected to active devices.

4. The invention as defined in claim 2 wherein said vias in said decoupling capacitor and the circuit board vias connected to said decoupling capacitor vias are each arranged in a straight line.

5. The invention as defined in claim 3 wherein said vias in said decoupling capacitor, and said vias in said I/C chip structure, and the circuit board vias connected to said decoupling capacitor vias, are each arranged in a straight line.

6. The invention as defined in claim 1 wherein each via in said decoupling capacitor connected to one circuit board via is completely surrounded by vias in said decoupling capacitor connected to another conductive plate.

7. The invention as defined in claim 1 wherein solder balls are provided to connect said decoupling capacitor to said circuit board.

8. A structure for reducing stray inductance in a circuit comprising:

a printed circuit board having first and second opposite faces and at least two voltage planes, and vias extending from each of said faces to one of said voltage planes,

an I/C chip structure having at least one active device thereon, connectors connecting said active devices on said I/C chip structure to said vias on one face of said printed circuit board,

a discrete decoupling capacitor structure comprising at least two interlaced conductive plates in dielectric material forming at least one capacitor connected to the other face of said printed circuit board,

vias extending from each of said conductive plates through said dielectric material to connect each via to a circuit board via on said second face of said printed circuit board,

said vias in said decoupling capacitor structure being configured and arranged such that the vias are parallel to each other, and each via connected to one conductive plate is located adjacent a via connected to another conductive plate.

9. The invention as defined in claim 8 wherein said vias in said printed circuit board are arranged in the same pattern as the vias in said decoupling capacitor.

10. The invention as defined in claim 9 wherein said I/C chip structure has vias therein arranged in the same pattern as the pattern of the vias in said decoupling capacitor, and each of said vias arranged in said pattern in said I/C chip structure being connected to active devices.

11. The invention as defined in claim 9 wherein said vias in said decoupling capacitor and the circuit board vias connected to said decoupling capacitor vias are each arranged in a straight line.

12. The invention as defined in claim 10 wherein said vias in said decoupling capacitor and the circuit board vias connected to said decoupling capacitor vias and the vias in said I/C chip structure are each arranged in a straight line.

13. The invention as defined in claim 8 wherein each via in said decoupling capacitor connected to one circuit board via is completely surrounded by vias in said decoupling capacitor connected to another conductive plate.

14. The invention as defined in claim 8 wherein solder balls are provided connecting said decoupling capacitor to said circuit board.

15. A structure for reducing stray inductance in a circuit comprising:

a printed circuit board having first and second opposite faces and at least two voltage planes, and vias extending from said one face to one of said voltage planes,

an I/C chip structure having first and second faces, and having at least one active device thereon, connectors connecting said active devices on said I/C chip structure through said first face of said I/C chip structure to said circuit board vias on said one face of said printed circuit board,

a discrete decoupling capacitor structure comprising at least two interlaced conductive plates in dielectric material forming at least one capacitor connected to said conductive plates of said I/C chip structure through said second face of said I/C chip structure,

vias extending from each of said conductive plates through said dielectric material to connect each via to a connector on said second face of said I/C chip structure,

said vias in said decoupling capacitor structure being configured and arranged such that the vias are parallel to each other, and each via connected to one conductive plate is located adjacent a via connected to another conductive plate.

16. The invention as defined in claim 15 wherein said I/C chip structure has vias therein arranged in the same pattern as the pattern of the vias in said decoupling capacitor, and each of said vias arranged in said pattern in said I/C chip structure being connected to active devices.

17. The invention as defined in claim 15 wherein said vias in said decoupling capacitor and said vias in said I/C chip structure are each arranged in a straight line.

18. The invention as defined in claim 15 wherein each via in said decoupling capacitor connected to one via in said printed circuit board is completely surrounded by vias in said decoupling capacitor connected to another conductive plate.

19. The invention as defined in claim 15 wherein solder balls are provided connecting said decoupling capacitor to said I/C chip structure.

20. A method for reducing stray inductance in a circuit comprising the steps of:

providing a printed circuit board having first and second opposite faces and at least two voltage planes, and vias extending from each of said faces to one of said voltage planes,

providing an I/C chip structure having at least one active device thereon; connectors connecting said active devices on said I/C chip structure to said conductors on one face of said printed circuit board,

providing a discrete decoupling capacitor structure comprising at least two interlaced conductive plates in dielectric material forming at least one capacitor, vias extending from each of said conductive plates through said dielectric material, said vias in said decoupling capacitor structure being configured and arranged such that the vias are parallel to each other, and each via connected to one conductive plate is located adjacent a via connected to another conductive plate, and

connecting each circuit board via to a decoupling capacitor on said second face of said printed circuit board.

21. The invention as defined in claim 20 wherein said vias in said printed circuit board are arranged in the same pattern as the vias in said decoupling capacitor.

22. The invention as defined in claim 21 wherein said I/C chip structure has vias therein arranged in the same pattern as the pattern of the vias in said decoupling capacitor, and each of said vias arranged in said pattern in said I/C chip structure being connected to active devices.

23. The invention as defined in claim 21 wherein said vias in said decoupling capacitor and the circuit board vias connected to said decoupling capacitor vias are each arranged in a straight line.

24. The invention as defined in claim 22 wherein said vias in said decoupling capacitor and the circuit board vias connected to said decoupling capacitor vias and the vias in said I/C chip structure are each arranged in a straight line.

25. The invention as defined in claim 20 wherein each via in said decoupling capacitor connected to one circuit board via is completely surrounded by vias in said decoupling capacitor connected to another conductive plate.

26. The invention as defined in claim 20 wherein solder balls are provided connecting said decoupling capacitor to said circuit board.

27. A method for reducing stray inductance in a circuit comprising the steps of:

providing a printed circuit board having first and second opposite faces and at least two voltage planes, and vias extending from said one face to one of said voltage planes,

providing an I/C chip structure having first and second faces, and having at least one active device thereon, connecting said active devices on said I/C chip structure through said first face of said I/C chip structure to said circuit board vias on said one face of said printed circuit board,

providing a discrete decoupling capacitor structure comprising at least two interlaced conductive plates in dielectric material forming at least one capacitor; vias extending from each of said conductive plates through said dielectric material to connect each via to a connector on said second face of said I/C chip structure,

said vias in said decoupling capacitor structure being configured and arranged such that the vias are parallel to each other, and each via connected to one conductive plate is located adjacent a via connected to another conductive plate, and

connecting said vias in said decoupling capacitor to the vias in said I/C chip structure.

28. The invention as defined in claim 27 wherein said I/C chip structure has vias therein arranged in the same pattern as the pattern of the vias in said decoupling capacitor, and each of said vias arranged in said pattern in said I/C chip structure being connected to active devices.

29. The invention as defined in claim 27 wherein said vias in said decoupling capacitor and said vias in said I/C chip structure are each arranged in a straight line.

30. The invention as defined in claim 27 wherein each via in said decoupling capacitor connected to one via in said printed circuit board is completely surrounded by vias in said decoupling capacitor connected to another conductive plate.

31. The invention as defined in claim 27 wherein solder balls are provided connecting said decoupling capacitor to said I/C chip structure.